# SOC 记



## CPU本纪

central

## GFX本纪

display

## NB本纪



### CPUIF世家

CPUIF is an interface connection module which connect CPU(HIF) and chipset. The main function is to transfer CDC interface with CPU to chipset internal interface with DRAMC （for C2M） and PXPTRF (for C2P and P2C).



### VPI世家

#### VPI MSGC列传

The Message Controller (MSGC) is designed to handle several kinds of messages, including Power Management message, NMI/SMI/SCI reporting.

The Message Controller will monitor the DLLM/PHY/PMU Condition in VPIL, Configuration Condition in VPIL CFG space, and then update the Configuration Status in VPIL CFG space, asserts NMI/SMI/SCI to NB, and also send Message to remote VPIL.



#### VPI LINK 列传

VPI is a connection media between two CPUs. VPI Link Layer, based on PCIE Data Link Layer, is the layer that basically transforms the data packets from CPU into a format for the Physical Layer. Other responsibilities of VPI Link Layer include link management, error detection, and error correction.

#### VPIL LPHY列传

VPI PHY is connected to DLLM, PMC, PHYES(EPHY), MSGC, and VPICFG. The connection diagram is as below.



（这里的PHYES就是VPI MSGC图中的EPHY）

#### VPIL PMU列传

VPIL PMC manages power of whole VPIL. It connects to DLLM, PHYLS, MSGC, and CFG. The connection diagram is as below.



### PXPTRF世家

PXPTRF is used to handle request and data transfer in NB, it acts as a traffic manager. In CHX002, it handles different cycles between PCIE, PEMCU, PCCA, VPI, MCA, SATA, GFX, TACTL, RAID0, RAID1, APIC and CPUIF. Otherwise, it connects to VKCFG by AHB protocol bus.

There are two types of transactions in current design:

* **Downstream cycle**. From CPU to PCIE, PCCA, **VPI,** MCA, XHCI, SATA, GFX. Include memory read/write, IO read/write, configuration and special cycle. (Blackbody bold means only downstream)
* **Upstream cycle**. From PCIE, **PEMCA,** PCCA, XHCI, SATA, GFX, **TACTL,** **RAID0, RAID1** to CPU. Include memory read/write cycles. (Blackbody bold means only upstream)
  + **Snoop cycle**: to make data consistency, upstream memory cycle should do snoop on Host CPU bus.
  + **Non-snoop cycle**: PXPTRF does not support non-snoop cycle in CHX002.
* **P2P cycle**. PXPTRF does not support p2p cycle in CHX002.



downstream和upstream，跟过不过PXP没关系。（图中像下的箭头表示downstream）

从CPU或其他源（如MCU）打下来cycle访问device的就是downstream（这里都要过PXPTRF）;

从device打出来的去CPU或者去DRAM，就是upstream。

### DRAMC世家

DRAM Controller is the interface module between NB and DRAM device. It communicates with DRAM according to the protocol of DDR4 device and ensures the AC timing on DRAM bus.

CHX002 memory interface will working modes:

Option1: Single 64-bit channel w/ or w/o ECC;

Option2: Dual 64-bit channel w/ or w/o ECC;

The interface between each DRAMC and other master in NB and DDR4 device is shown as below:



SOCCAP

(XHCI)

MCUTRF

(AZALIA)

DRAMC CORE Figure as below:



### DDRIO世家

完成CLOCK domain的转换；



### GMINT世家

GMINT is a Graphic request control module and it connects our Internal Graphic and DRAM controller.

In CHX002, there will be two channel DRAMC, so two symmetrical GMINT will be used to connect each DRAMC, they are GMINTA and GMINTB. This two GMINT are completely independent as shown as below:



### RAIDA世家

RAID0 and RAID1.

RAIDA -- Redundant Arrays of independent Disks Accelerator. It supports XOR/non-zero/memory copy/memory compare/memory filled/Reed Solomon Codec/CRC16 generator/Function Level Reset operation. It executes above operation basing on descriptor. As show as below, it connects to PXPTRF, and has two independent channels. Its configurable registers are in VKCFG. By the way, it also has interfaces with VKCFG.



### TACTL世家

CHX002 will implement the virtualization technology for directed I/O（VIO）. so the hardware architecture must change for DMA remapping and interrupt remapping. (The detail information of this part, please refer to the spec of “Intel Virtualization technology for Directed I/O”).

TA controller is the hardware design implement in NB. According to the spec, it will do the DMA address remapping, interrupt remapping, cache invalidation and fault reporting when error detected.

The device under NB can be divided to two types: PCIE device and SB/AHCI/XHCI/GFX/RAIDA device. For PCIE device, when there’s DMA cycle pending, PCIE will hold it firstly and issue the request for address remapping to TA controller, after the remapped address returned, PCIE will flush this DMA cycle to PXP with the physical address. So for PCIE device, the DMA request input to PXP is all with the physical DRAM address after remapped. For SB/AHCI/XHCI/GFX/RAIDA device, PXP will help to handle the address remapping, SB device issue the DMA cycle with the virtual address to traditional PXP, PXP will hold the request firstly and then issue the address remapping request to TA controller, after PXP get the remapped address, it will issue upstream request to DRAM with the physical address.



### PCIE世家

#### PCIE TRANS列传

CHX002 has eight PCI Express (PCIE) ports. These eight ports make up of PCIE Controller (PEXC), which is the PCIE Root Complex from the point of view of PCIE topology. All ports are compatible to the PCI Express 3.0 Base Specification. This document focuses on PCIE TRANS design.

PCIE is composed of three logical layers: Transaction Layer (TRANS), Data Link Layer (DLLM) and Physical Layer (PHY). The primary responsibility of TRANS is assembly of Transaction Layer Packet (TLP) in downstream path and disassembly of TLP in upstream path.

In downstream path, TRANS receives downstream read/write request from PCIE Arbitration Controller (PEARB) or message request from Message Controller (MSGC), and then generates downstream request TLP to DLLM. It also generates downstream completion TLP to DLLM when the read data for upstream read request is back from PEARB.

In upstream path, it receives upstream TLP from DLLM, translates it into read/write requests to PEARB, message signals to MSGC, MSGC MSI request and sends it to PEARB or interrupt signals to Advanced Programmable Interrupt Controller (APICX). When TRANS receives an upstream completion TLP, it will complete the downstream non-posted request.

Besides, TRANS also ensures transaction ordering, tracks flow control credits and exchange credit status with remote PCIE device periodically.



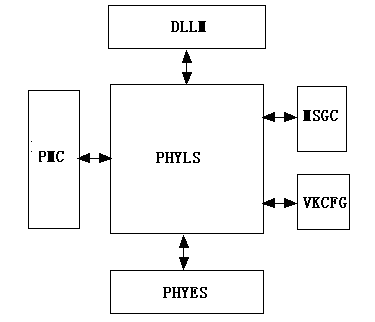
#### PCIE DLLM列传

Data Link Layer is the middle layer in the PCI Express stack, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.



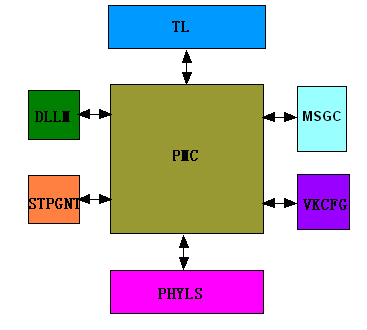
#### PCIE PHY列传

PCIE PHY is a layer of PCI Express. It is connected to DLLM, PCIE\_PMC, PHYES, MSGC, and VKCFG. The connection diagram is as below.



#### PCIE PMU列传

PCIE PMU isn’t a layer of PCI Express. Power management is an independent function in PCI Express. It manages power of whole PCIE, but main in PHY. It is connected to TL, DLLM, PHY, MSGC, STPGNT and VKCFG. The connection diagram is as below.



### PEMCU世家

PEMCU (The module name of R8051XC2 In CHX002 for PEXC) is used for Gen3 Equalization.

Upstream with PXPTRF.

Downstream with PCIE CFG and VPIL CFG.



### APIC世家

Advanced programmable interrupt controller.

NB APICX is designed to transfer NB’s PCIE, EUMA , RAIDA and MSGC’s interrupt to MSI cycle, and send to CPU, when system work in APIC mode.

When system working in PIC mode, NB APICX will transfer NB’s PCIE, EUMA, RAIDA and MSGC’s interrupt to SB through “NB2SB\_INTA~NB2SB\_INTD”, “NB2SB\_INTA~NB2SB\_INTD” will connect to SB side 8259. This signal will be an output pin connect to SB.

Another function is in APIC mode, when a MSI cycle send through APIC, APICX will trigger NB2SB\_APIC\_WAKE signal to notice SB PMU module, when the CPU in the C2/C3/C4/C5/C6 mode, we should wake it up. When there is MSI cycle pending in PXPTRF, APICX will driver NB2SB\_PEND\_MSI signal to SB.



### MCUTRF世家（列传）

为SB device的non-snoop cycle量身定制的，比如HDAC (AZALIA)，但在未来很可能消失，如果没有SB device support non-snoop的话。

MCUTRF is used to handle non-snoop request and data transfer in NB, it connects XHCIMCU, AZALIA and DRAMC

In CHX003, there will be two master sending request to access DRAM, so request from XHCIMCU and Azalia will be temporary stored in request queue before MCUTRF doing arbitration to send out request. This structure of MCUTRF is shown as below:



### SOCCAP世家（列传）

SOCCAP (SOC Capture) is a customized version of FSBC (FSB Capture) for SOC chip. It contains all FSBC’s functions except capturing FSB signals because there is no FSB in SOC chip. Note that both FSBC and SOCCAP are existent in CHX002 where FSBC is in CPU and SOCCAP is in NB. FSBC will capture debug signal in CPU side and SOCCAP will capture debug signal in NB or SB side. They can work independent or associated depend on different work mode.

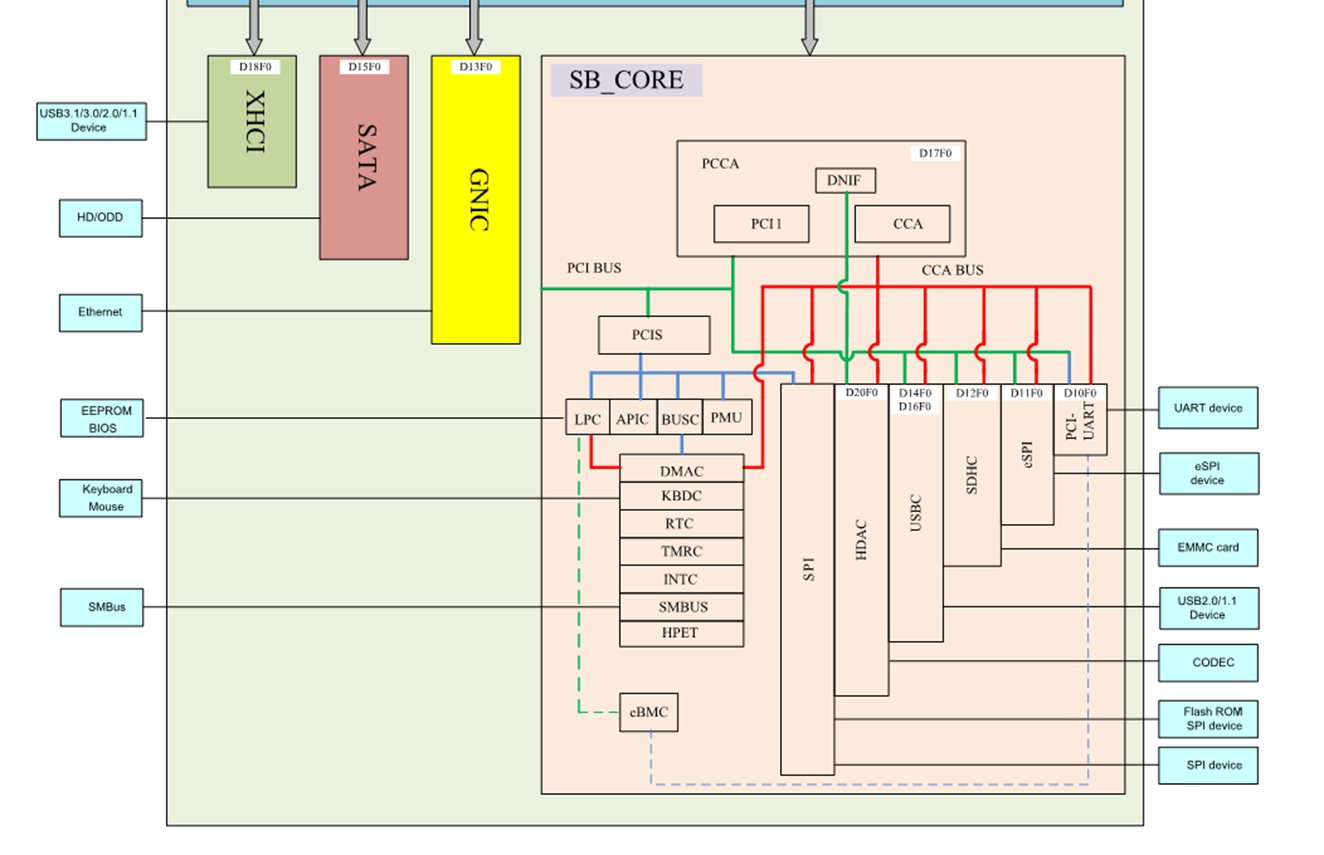
SOCCAP enhances the function of capturing debug signals and uses debug signals as trigger condition. Theoretically, SOCCAP can restore any waveform on any bus if only the bus signals are included in ASIC debug signal group.

（注：CPU和Chipset的Interface被称为FSB）

The below figure shows the position of SOCCAP in system. SOCCAP can capture two ASIC debug signal groups at the same time, then packet the signals and send them to DRAM or PCIE. SOCCAP also can send out downstream request to PXPTRF controlled by MCU or JTAG. In CHX002, XHCI MCU will be the master of SOCCAP.



## SB本纪



### PCCA世家

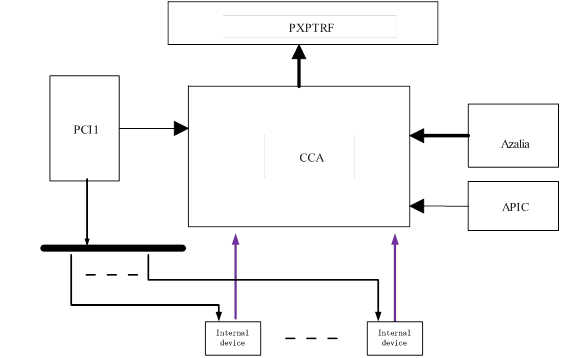
The role of PCCA in CHX002 is to manage the data flow between its four interfaces and NB for upstream cycles. The four interfaces are:

1) internal devices ( internal devices including legacy devices, HPET, UHCI and EHCI, ESPI, SPI, PCI-UART),

 2) PCI1,

 3) AZALIA,

 4) Interrupt and system management cycle.



### XHCI世家

连接USB3

USB3HC is an internal SB device, which is used as USB3.0 Host Controller. It complies with the Universal Serial Bus 3.0 Specification and Intel’s eXtensible Host Controller Interface (xHCI R1.1), and is fully backward compatible with USB 2.0 and USB 1.1 specifications, ensuring seamless connectivity of legacy USB devices.

USB3HC in CHX002 could support 2 USB SS Root Ports and 2 USB2 Compliance Root Ports. And another two USB2.0 Host Controller (D16 + D14), D16 (EHCI + 2 UHCI) support 4 USB2 Compliance Root Port , D14(1EHCI + 1UHCI) support 1EHCI and 1UHCI support 2 USB2 Compliance Root Port.



### SATA世家

SATA: Serial ATA Host Controller.

ATA: Advanced Technology Attachment. (高级技术附件)

连接硬盘 （AHCI）

SATA AHCI: SATA接口的工作模式之一，此外还有RAID和IDE。

该模式全称：Serial ATA Advanced Host Controller Interface. 串行ATA高级主控接口。

RAID: Redundant Array of Independent Disk. 独立冗余磁盘阵列

The spec gives a brief introduction to the SATA design in CHX002 project. There is one SATA HBA working as PCI Devices: Device 15 Function 0 with 2 ports.

The SATA downstream and upstream interface in connected to PXPTRF interface and both the two SATA Devices share one downstream/upstream interface.

There is one EPHY for SATA: with 2 SATA ports and shared with PCIE.

PXPTRF

SB\_CORE

SATA

SATA\_CORE

STRFDN

STRFUP

PHYD\_CFG

PHYD\_INTF

PLLC\_PHYD

SACFGREG

RST\_CENTER

SCKGRP

SATOPDBG

SASUBDBG

GHC

SA\_EPHY\_TST

PIOCA

SAPORT0

AHCICTL

AHDMAC

AHTP

LINK\_PHY

SAFIFO(PG)

SACTL

SADMAC

SATP

SAPORT1

AHCICTL

AHDMAC

AHTP

LINK\_PHY

SAFIFO(PG)

SACTL

SADMAC

SATP

SATA\_TXCDC

SATA\_EPHY

Port0

PORT1

### HDAC世家(AZALIA)

AZALIA，播音录音，音频解码

HDAC communicates with external CODEC through High Definition Audio serial link. HDAC moves samples of digitally encoded data between system memory and an external CODEC(s) through DMA engine. In CHX002, HDAC implements four output DMA engines and four input DMA engines. The output DMA engines move digital data from system memory to CODEC D-A converter. HDAC implements serial data output signal (AZSDO), AZSDO is connected to external CODEC. The input DMA engines move digital data from the A-D converter in the CODEC to system memory. In a CHX002 system, it only needs two AZSDIs. HDAC combines output DMA engines and input DMA engines together as one engine, An arbiter decides which DMA request will be executed. Figure 1-1 is CHX002 HDAC Block Diagram.



**Figure 1‑1 High Definition Audio Architecture Block Diagram**

SB\_CORE

Internal device

DNIF

PCI1

CCA

PCCA

**HDAC**

PXPTRF

PCI bus

**HDAC downstream**

**interface**

**HDAC snoop upstream**

**Interface**

CODEC

**HD Audio Link**

**HDAC non-snoop upstream**

**interface**

### USB2世家

### PMU世家

### RTC/LPC世家

### I2C/SPI世家

附录：

DDR带宽：

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| SDRAM/DDR | 型号 | 数据位宽 | 内部MHZ | 频率速度 | 带宽 |
| SDRAM | PC100 | 64 | 100 | 100 | 800MB/s |
| SDRAM | PC133 | 64 | 133 | 133 | 1064MB/s |
| DDR | DDR-266 | 64 | 133 | 266 | 2.1GB/s |
| DDR | DDR-400 | 64 | 200 | 400 | 3.2GB/s |
| DDR | DDR2-800 | 64 | 200 | 800 | 6.4GB/s |
| DDR | DDR3-1600 | 64 | 200 | 1600 | 12.8GB/s |

注：标红处表示DDR, DDR2, DD3分别支持2预取，4预取和8预取。

DDR4-3200: 25.6GB/s

PCIe带宽：

|  |  |  |
| --- | --- | --- |
| 规格 | 1x带宽 | 16x带宽 |
| PCIe1.0 | 250MB/s | 4GB/s |
| PCIe2.0 | 500MB/s | 8GB/s |
| PCIe3.0 | 约1GB/s | 约16GB/s |
| PCIe4.0 | 约2GB/s | 约32GB/s |

PCIe是显卡的规格，由PCI升级AGP, 再由AGP升级而来。显卡又称为VGA（Video Graphics Array）,主要通过GPU的控制芯片来与CPU、内存等通信。

SATA带宽：

|  |  |  |
| --- | --- | --- |
| 版本 | 带宽（Gbit/s） | 速度（MB/s） |
| SATA1.0 | 1.5 | 150 |
| SATA2.0 | 3 | 300 |
| SATA3.0 | 6 | 600 |

SATA的带宽计算上，10bits=1B。因为当传输10bits编码时，仅有8bits为数据，其余2bits为检验只用。

磁盘速度：80~120MB/s（240MB/s）

固盘速度（FLASH）：500MB/s (极限)

U盘速度：

|  |  |  |
| --- | --- | --- |
| 版本 | 带宽（Mbit/s | 速度（MB/s） |
| USB1.0 | 12 | 1.5 |
| USB2.0 | 480 | 60 |
| USB3.0 | 5G | 500 |
| USB3.1 | 10G | 1000 |

注：在主板上，USB的实际速度可能要减半。